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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/186,584	11/05/1998	JAMES D. GREENFIELD	EN998073	1986

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EXAMINER
LEE, RICHARD J

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 04/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/186,584	Applicant(s) Greenfield et al
	Examiner Richard Lee	Art Unit 2613

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 12, 2001* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-35* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

1. The request filed on October 12, 2001 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/186,584 is acceptable and a CPA has been established. An action on the CPA follows.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-6, 16-19, 32, and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Greenfield et al of record (5,760,836).

Greenfield et al discloses a FIFO feedback and control for digital video encoder as shown in Figures 1 and 5, and the same method and encoder as claimed in claims 1-6, 16-19, 32, and 34 for encoding a digital video image stream in the encoder (see Figure 1), comprising means (21 of Figure 1) for spatial compression of still images in the digital video image stream and means (41 of Figure 1) for temporal compression between the still images, wherein the means for spatial compression comprises means for converting a time domain image of a macroblock to a frequency domain image of the macroblock (see column 1, lines 55-63), means for taking a discrete cosine transform of the frequency domain image (see column 1, lines 55-63), means for transforming the discrete cosine transformed macroblock image by a quantization factor (see 23 of Figure 1), and means for run length encoding the quantized discrete cosine transformed macroblock image (see

25 of Figure 1), wherein the means for temporal compression comprises means for reconstructing the quantized, discrete cosine transformed image of the macroblock (see Figure 1), means for searching for a best match macroblock, and means for constructing a motion vector therebetween (see column 6, line 55 to column 7, line 11), the encoder for encoding thereby forming a bitstream comprising run length encoded, quantized, discrete cosine transformed macroblocks and motion vectors and passing the bitstream to and through an external buffer to a transmission medium (see column 6, line 55 to column 7, line 11), comprising means for feeding back to hardware logic (i.e., as provided by the buffer management system of Figure 5) within the encoder an external read signal from a host (see 51 and FIFO_RD of Figure 5, and columns 5-7), and for incrementing an on-chip counter of the hardware logic each time that the external buffer is read and calculating therefrom the number of bits read by a host (see column 5, lines 31-50), the hardware logic in the encoder being further adapted to monitor a number of bits encoded and written into the external buffer and subtract from the number of bits encoded the number of bits read by the host to continuously obtain the real time fullness of an external buffer, wherein the continuously obtaining comprises obtaining the real time fullness of the external buffer every cycle of the encoder (i.e., by having a real time encoding system, real time fullness of the external buffer is maintained every cycle of the encoder, see column 1, lines 32-49, column 5, lines 24-30, lines 53-59), and wherein the hardware logic in the encoder is further adapted to provide the host with a dynamic buffer level indicator in real time indicative of the fullness of the external buffer (see columns 5-7); wherein the logic adapted to provide the host with a dynamic buffer level indicator comprises

logic adapted to continuously compare the real time fullness of the external buffer (i.e., by having a real time encoding system, real time fullness of the external buffer is maintained, see column 1, lines 32-49, column 5, lines 24-30, lines 53-59), with a buffer threshold defined by the host and to provide a high level indicator when the buffer fullness is greater than the buffer threshold and a low level indicator when the buffer threshold is greater than the buffer fullness (see column 6, lines 18-29); further comprising a buffer threshold register (153 of Figure 5) within the encoder coupled to the logic adapted to compare the buffer fullness to the buffer threshold, wherein the external buffer comprises at least one FIFO buffer (see column 1, column 6, lines 18-45, and Figure 5); an external buffer configuration register (151 of Figure 5) in the encoder for retaining multiple external buffer configuration values, and wherein the calculating in the encoder the number of bits read by the host includes employing a predefined configuration value of the external buffer configuration register in determining the number of bits read by the host upon receipt of each buffer read signal from the host, and wherein the multiple external buffer configuration values retained in the external buffer configuration register comprise at least some of 1, 2, 4, and 8 byte buffer configuration values, each value being representative of a number of bytes read from the external buffer with each buffer read signal from the host for a respective external buffer configuration (see column 5, lines 31-50).

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 7-15, 20-31, 33, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greenfield et al as applied to claims 1-6, 16-19, 32, and 34 in the above paragraph (3), and further in view of Choe et al of record (6,094,696).

Greenfield et al discloses substantially the same method and encoder for encoding a digital video image stream in the encoder as above, further including wherein the external buffer comprises one of a field buffer or cascaded FIFO buffers (see Figure 5), continuously comparing the fullness of the external buffer to a predefined buffer size and providing the host with a high level indicator when the buffer fullness is greater than or equal to the buffer size and a low level indicator when the buffer size is greater the buffer fullness, and providing an on chip buffer size register for holding a host defined buffer size value for use in the comparing of the buffer fullness to the buffer size (see columns 5-6).

Greenfield et al does not particularly disclose, though, providing from the encoder to the host in real time a dynamically updated flag comprising at least one of a buffer empty flag, a buffer almost full flag and a buffer full flag as claimed in claims 7-11, 13, 20-22, 24, 27, and 29-31. However, Choe et al discloses a virtual serial data transfer mechanism and teaches the conventional use of a buffer management system wherein buffer full and buffer empty flags are set

(see column 2, line 62 to column 3, line 56). Therefore, it would have been obvious to one of ordinary skill in the art, having the Greenfield et al and Choe et al references in front of him/her and the general knowledge of flag indicating statuses for a buffer management system, would have had no difficulty in providing the dynamic buffer flagging system as taught by Choe et al as part of the buffer management within Figure 5 of Greenfield et al for the same well known flag identification purposes as claimed.

6. Regarding the applicants' arguments at pages 16-20 of the amendment filed September 17, 2001 concerning in general that "... Greenfield et al specifically describes a non-real time buffer level indicator. In Greenfield et al the buffer level indicator is provided dependent upon how often the processor updates the indicator. The hardware described in Greenfield et al would be incapable of supporting any real time application .. the microcode reads the register and compares it with the buffer fullness in bytes (BF/8). This means that the processor is doing the updating of the buffer level indicator and that the buffer level signal is not returned on a real time basis ... Real time encoding is different from and independent of applicants' recited real time monitoring of external buffer fullness ...", the Examiner respectfully disagrees. It is submitted that at column 5, lines 24-30, Greenfield et al teaches that real time encoding systems typically use an external FIFO buffer device for the adjustment of quantization step sizes. As such, it is clear and inherent that the real time monitoring of the external buffer fullness is not independent from the real time encoding system. And since these processings and monitorings of the external buffers are provided in real time as taught by Greenfield et al, applicants' arguments that the microcode

implementation of Greenfield comprises a non-real time implementation is not convincing. If the external buffer fullness of Greenfield et al is not being monitored in real time, then how else would the encoding system of Greenfield et al as a whole be provided in real time. In other words, for the encoding system of Greenfield et al to be provided in real time as described at column 5, lines 24-30, all components/processings within the encoder must inherently be performed in real time as well.

Regarding the applicants' arguments at pages 20-25 of the amendment filed September 17, 2001 concerning in general that "... Applicants respectfully submit that this passage does not identify an adequate teaching, suggestion or incentive in the art itself to combine these references as required by Winner & Arkie, but rather simply restate the ultimate result of the combination in a conclusory manner without any underlying reasoning supporting the combination ... Neither Greenfield et al nor Choe et al provide from an encoder to a host a dynamically updated flag in real time. In fact, applicants not that Choe et al does not even involve an encoding process ...", the Examiner respectfully disagrees. The Examiner wants to point out that the combination rejection is not simply restating results of the invention from applicants' specification as argued, but instead is based on the specific teachings of the combination of Greenfield et al and Choe et al as provided in the above paragraph (5). In addition, Choe et al describes many applications for the buffer management circuit which includes real time processings of multimedia having video and audio components, video capture and playback, etc. (see column 1, lines 18-40), and it is considered obvious that encoded video data may be provided as part of the multimedia

applications. The applicants are reminded that: One of ordinary skill in the art is presumed to possess a certain amount of background knowledge independent of the references. In re Sovish, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985); In re Jacoby, 309 F.2d 513, 135 USPQ 317 (C.C.P.A. 1962). The conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Bozek, 416 F.2d 1385, 163 USPQ 545 (C.C.P.A. 1969). As such, it is submitted again that the dynamic buffer flagging system as taught by Choe et al may certainly be provided as part of the buffer management within Figure 5 of Greenfield et al for the same well known flag identification purposes as claimed.

7. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications intended for entry)

(for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Lee whose telephone number is (703) 308-6612. The Examiner can normally be reached on Monday to Friday from 8:00 a.m. to 5:30 p.m, with alternate Fridays off.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group customer service whose telephone number is (703) 306-0377.

RICHARD LEE
PRIMARY EXAMINER

Richard Lee/rl

4/5/02